Course Handout for 04 Years B.Tech PROGRAM

Name of the Faculty: Subrata De
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Course Title	: Computer Architecture
Course Code	: PCC-CS402
L-T-P-S Structure	: 3-0-3-0
Credits	: 3
Pre-requisite	: NA
Course Coordinator	: Subrata De

Course Objective:

1. To understand the principles of pipelining.
2. To understand various architecture like superscalar architecture, VLIW architecture.
3. To learn the concept of multiprocessor architecture.
4. To understand the applications of the theories taught in the subject. This will be achieved through the project and some selected lab sessions.

COURSE OUTCOMES (COs):

CO No.	Course Outcome (CO)	Blooms Taxonomy Level (BTL)	Target %
PCC-CS402.1	**Understand** pipelining concepts with a prior knowledge of stored program methods.	Level-2	65%
PCC-CS402.2	**Understand** the concepts of data hazards, control hazards and structural hazards, techniques for handling hazards.	Level-2	65%
PCC-CS402.3	**Understand** different memory hierarchy and mapping techniques.	Level-2	65%
PCC-CS402.4	**Understand** Instruction-level parallelism concepts.	Level-2	65%
PCC-CS402.5	**Explain** multiprocessor architecture and interconnection network.	Level-2	65%

PROGRAM OUTCOMES (POS):

1. **Engineering Knowledge**	Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.
2. **Problem Analysis**	Identify, formulate, review research literature, and analyse complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.
3. **Design / development of solutions**	Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.
4. **Conduct investigations of complex problems**	Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.
5. **Modern tool usage**	Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modelling to complex engineering activities with an understanding of the limitations.
6. **The engineer and society**	Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.

7. **Environment and sustainability**	Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.
8. **Ethics**	Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.
9. **Individual and team work**	Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.
10. **Communication**	Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.
11. **Project management and finance**	Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.
12. **Lifelong learning**	Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

Mapping of Course Outcomes and Program Outcomes:

Course Outcomes	Program Outcomes												PSOs		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
PCC-CS402.1	1	2	-	-	-	-	-	-	-	-	-	-	1	2	1
PCC-CS402.2	1	1	-	-	-	-	-	-	-	-	-	-	1	2	1
PCC-CS402.3	1	1	-	-	-	-	-	-	-	-	-	-	1	2	1
PCC-CS402.4	1	-	-	-	-	-	-	-	-	-	-	-	1	2	1
PCC-CS402.5	1	1	-	-	-	-	-	-	-	-	-	-	1	2	1
PCC-CS402	1	1	-	-	-	-	-	-	-	-	-	-	1	2	1

1 = courses in which the student will be exposed to a topic
2 = courses in which students will gain competency in that area
3 = courses in which students will master that skill

SYLLABUS (MAKAUT):

Unit	Content	Hrs.
1	Introduction : Review of basic computer architecture, Quantitative techniques in computer design, measuring and reporting performance, Pipelining: Basic concepts, instruction and arithmetic pipeline, data hazards, control and structural hazards, techniques for handling hazards, Exception handling. Pipeline optimization techniques; Compiler techniques for improving performance.	12
2	Hierarchical memory technology: Inclusion, Coherence and locality properties; Cache memory organizations, Techniques for reducing cache misses; Virtual memory organization, mapping and management techniques, memory replacement policies.	08
3	Instruction-level parallelism: basic concept, techniques for increasing ILP, superscalar, superpipelined and VLIW processor architectures. Array and vector processors.	06
4	Multiprocessor architecture: taxonomy of parallel architectures; Centralized shared- memory architecture: synchronization, memory consistency, interconnection networks. Distributed shared memory architecture. Cluster computers. Non von Neumann architectures: data flow computers, reduction computer architectures, systolic architectures.	07

TEXT BOOKS (T):

1. "Computer Organization and Architecture", T. K. Ghosh, A. J. Pal, Tata McGraw Hill Publishers.
2. "Computer Architecture A Quantitative Approach", J. L. Hennessy, D. A. Patterson, Morgan Kauffman Publishers.

COURSE DELIVERY PLAN:

Week	Topic (s)	CO	Book No., [Ch. No.], [Pg. No.]	Teaching-Learning Methods	Planned Date	Execution Date
1	Introduction: Background, Review of basic computer architecture, Quantitative techniques in computer design	1	T1, [1], [1,4,9]	T: Chalk & Talk L: Observes understands	04/01, 09/01	
2	Measuring performance of computer	1	T1, [8], [2]	T: Questioning / Discussion L: Answering questions, Participates	10/01, 11/01	
	Pipelining: Basic concepts, Instruction and arithmetic pipeline.	1	T1, [8], [8-12]	T: Chalk & Talk L: Observes understands	16/01, 17/01	
3	Data hazards, structural hazards	2	T2, [8], [19-20]	T: Lecturing L: Observes understands	18/01, 24/01	
	Control hazards and how it happens, Techniques for handling hazards	2	T1, [8], [17-21]	T: Chalk & Talk L: Observes understands	30/01, 31/01	
4	Exception handling, Pipeline optimization techniques, Compiler techniques for improving performance	2	PPT and Web source	T: PPT L: Observes understands	01/02, 06/02	
5	Hierarchical memory technology: Inclusion, Coherence, Spatial locality and temporal locality properties.	3	PPT and Web source	T: PPT L: Observes understands	07/02, 08/02	
6	Cache memory organizations, Techniques for reducing cache misses, Virtual memory organization.	3	T1,[4],[22-30]	T: Chalk & Talk L: Observes understands	13/02, 14/02, 15/02	
7	Mapping and management techniques, Memory replacement policies, Instruction-level parallelism: basic concepts.	3	T1,[4],[23-27] T2, [3],[148]	T: Chalk & Talk L: Observes understands	20/02, 21/02	
8	Techniques for increasing ILP, Superscalar,superpipelined architecture, VLIW processor architectures	4	T1,[8],[22-24] T2, [3], [192]	T: Chalk & Talk L: Observes understands	22/02, 27/02	
9	Basic concept of Array processors, Concept of vector processors.	4	T1,[8],[24-28]	T: Chalk & Talk L: Observes understands	28/02, 01/03	
	Multiprocessor architecture concept.	5	T1,[8],[37]	T: Chalk & Talk L: Observes understands	06/03, 07/03, 08/03	

10	Taxonomy of parallel Architectures, Centralized shared- memory architecture concept, Synchronization, memory consistency.	5	T1,[8],[1] T1,[8],[39]	T: Chalk & Talk L: Observes understands, Problem solving	13/03, 14/03, 15/03	
11	Interconnection networks, Distributed shared memory architecture.	5	T1,[8],[36-37]	T: Chalk & Talk L: Observes understands	20/03, 21/03, 22/03	
	Cluster computers.	5	T1,[8],[32]	T: Chalk & Talk L: Observes understands	27/03, 28/03	
12	Non von Neumann architectures concept , Data flow computers.	5	T1, [8],[36]	T: Chalk & Talk L: Observes understands	29/03, 03/04	
	Systolic architectures, Reduction computer architectures.	5	T1, [8],[6] T2, [3], [155]	T: Chalk & Talk L: Observes understands	04/04, 05 /04	

WEEKLY HOMEWORK ASSIGNMENTS/ PROBLEM SETS/OPEN ENDEDED PROBLEM-SOLVING EXERCISES etc.

Week	Assignment/Quiz	Topic	Details	CO
2	A01	Instruction Pipeline	Explain how speedup k can be achieved in k-stage instruction pipeline.	CO1
5	A02	Pipeline Hazard	Explain various types of data hazard problem.	CO2
7	A04	VLIW & Superscalar Architecture	Differentiate between VLIW & Superscalar Architecture. Explain how CPI value less than 1 can be achieved.	CO4
12	A03	Multi-processor	Explain cache coherence problem. How snoopy protocol works to solve cache – coherence problem.	CO5

COURSE TIME TABLE:

Class/Day	Monday	Tuesday	Wednesday
Theory	02:10 PM – 03:00 PM (01 Periods)	10:50 AM – 11:40 AM (01 Periods)	11:40 AM – 12:30 PM (01 Period)

REMEDIAL CLASSES:

Supplement course handout, which may perhaps include special lectures and discussions that would be planned, and schedule notified accordingly.

EVALUATION: AS PER MAKAUT GUIDELINES

Schedule for Continuous Assessment (CA)

CA	Assessment By	Schedule
CA-I	Presentation, Quiz, Group Discussion (25 Marks)	01.02.23 – 04.02.23
CA-II	Report writing (25 Marks)	01.03.23 – 04.03.23
CA-III	Class test in pen and paper mode to be conducted at the College Level (25 Marks)	01.04.23 – 04.04.23
CA-IV	Centralized online test to be arranged by the University (25 Marks)	01.05.23 – 04.05.23

ATTENDANCE POLICY

Every student is expected to be responsible for regularity of his/her attendance in class rooms and laboratories, to appear in scheduled tests and examinations and fulfil all other tasks assigned to him/her in every course. For Promotion, a Minimum of 50% of internal marks must be obtained. In every course, student has to maintain a minimum of 75% attendance to be eligible for appearing in Semester end examination of the course, for cases of medical issues and other unavoidable circumstances the students will be condoned if their attendance is between 60% to 75% in every course, subjected to submission of medical certificates, medical case file and other needful documental proof to the concerned departments.

DETENTION POLICY

In any course, a student has to maintain a minimum of 75% attendance and must secure a minimum of 50% marks in In-Semester Examinations to be eligible for appearing to the Semester End Examination, failing to fulfill these conditions will deem such student to have been detained in that course.

PLAGIARISM POLICY

Use of unfair means in any of the evaluation components will be dealt with strictly, and the case will be reported to the examination committee.

COURSE TEAM MEMBERS, CHAMBER CONSULTATION HOURS AND CHAMBER VENUE DETAILS:

S.No.	Name of Faculty	Chamber Consultation Day (s)	Chamber Consultation Timings for each day	Chamber Consultation Room No	Signature of Course faculty
01	Subrata De	As per prior appointment		Faculty cubicle	

GENERAL INSTRUCTIONS

Students should come prepared for classes and carry the text book(s) or material(s) as prescribed by the Course Faculty to the class.

NOTICES

All notices will be communicated through the institution email.

All notices concerning the course will be displayed on the respective Notice Boards.

Subrata De

Signature of COURSE COORDINATOR:

HEAD OF DEPARTMENT:

Principal
Sikkim Institute of Technology

Approval from: Head of the Institutions
(Sign with Office Seal)